

with the conditional instruction reveals that output of the subgraph will not be selected.

## **REMARKS**

### **I. Introduction**

Claims 179 to 181 and 183 to 203 are currently pending in the present application, since claims 1 to 178, and 182 were previously canceled. In view of the foregoing amendments and the following remarks, it is respectfully submitted that all of the presently pending claims are allowable, and reconsideration of the present application is respectfully requested.

Applicants thank the Examiner for the indication that the objections raised in the Office Action dated March 28, 2006 to the drawings, specification, and claims have been withdrawn.

Applicants thank the Examiner for considering the previously filed Information Disclosure Statements, 1449 papers, and cited references.

### **II. Support for Features of Claims 179 to 181, and 203**

The Examiner requests that Applicants show where in the application as originally filed there is support for the features previously included in canceled claim 182 which were added to each of claims 179 to 181 in the Amendment dated September 28, 2006. Support for these features may be found in original claim 2. In this regard, it is noted that the originally filed claims themselves are part of the specification. See MPEP § 2163(I)(A).

Furthermore, as the Examiner points out, the Specification, e.g., at page 7, refers to minimizing signals between subgraphs. Minimization of signals occurs where processing cells configured in accordance with the subgraphs provide signals to each other in accordance with the subgraphs. With respect to the subgraphs themselves, however, the signals between subgraphs are represented as connections. Accordingly, the discussion in the Specification regarding minimization of signals between subgraphs, *i.e.*, between cells configured in accordance with the subgraphs, provides support for minimization of connections between subgraphs.

The Examiner requests that Applicants show where in the application as originally filed there is support for the features of claim 203 added in the Amendment dated September 28, 2006. Support for these features may be found in the Specification, e.g., at page 56, line 33 to page 57, line 13.

### III. Claim Objections

While Applicants do not necessarily agree with the objections to claims 179 to 181 and 203, to facilitate matters, these claims have been amended herein without prejudice to obviate the present objections.

Withdrawal of the present objections is therefore respectfully requested.

### IV. Rejection of Claims 179, 181, 185, 187, and 188 Under 35 U.S.C. § 102(e)

Claims 179, 181, 185, 187, and 188 stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,966,534 (“Cooke et al.”). It is respectfully submitted that Cooke et al. do not anticipate any of claims 179, 181, 185, 187, and 188 for at least the following reasons.

Claim 179 relates to a method for programming a system having a cellular structure and recites, *inter alia*, the following:

*... separating the control flow graph into a plurality of subgraphs;  
and distributing the plurality of subgraphs among a plurality of  
programmable hardware modules; wherein the separating includes  
separating the control flow graph so as to minimize connections  
between the plurality of subgraphs.*

The Office Action asserts that Cooke et al., at column 5, lines 31 to 41 and column 6, lines 9 to 18 discloses these features. With respect to column 5, lines 31 to 41, the cited section merely indicates that loops are independent. While the loops may be represented as a control graph, Cooke et al. do not disclose that such a control graph is separated according to the loops, where the subgraphs are distributed among hardware modules. Indeed, the cited section is not at all related to separating a control flow graph into a plurality of subgraphs, and certainly does not disclose a particular way to perform such separating.

Further, to the extent that the Office Action may be relying on the doctrine of inherent disclosure, the Office Action must provide a “basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics necessarily flow from the teachings of the applied art.” (See M.P.E.P. § 2112; emphasis in original; *see also Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)). It is respectfully submitted that the criteria for obviousness have not been satisfied. In this regard, while the loops are indicated to be “generally independent,” they are not always independent. Thus, even if the control graph which may represent the loops would be separated according to the loops (which Cooke et al. do not disclose), the lack of connections

between the subgraphs does not inhere in such a separation. Accordingly, separation of the control flow graph into subgraphs according to the loops (which is not disclosed) does not disclose, or even suggest, the features of separating a control flow graph into a plurality of subgraphs, where the separating includes separating the control flow graph so as to minimize connections between the plurality of subgraphs.

With respect to column 6, lines to 18, the cited section is unrelated to the features of separating a control flow graph so as to minimize connections between subgraphs. The cited section merely indicates that, after functions are assigned to various FPGA blocks, the functions are scheduled.

Further, with respect to the division and distribution of tasks over the various FPGA blocks in Cooke et al., the division and distribution are indicated to be based on equalizing lengths of time of processing by the FPGA blocks; they are not performed minimize connections. See Cooke et al., column 5, line 5 to column 6, line 8.

Thus, Cooke et al. do not disclose, or even suggest, all of the features recited in claim 179. Accordingly, Cooke et al. do not anticipate claim 179.

Claim 181 includes subject matter similar to that of claim 179. It is therefore respectfully submitted that Cooke et al. do not anticipate claim 181 for essentially the same reasons as set forth above in support of the patentability of claim 179.

As for claims 185, 187, and 188, which depend from claim 181 and therefore include all of the features recited in claim 181, it is respectfully submitted that Cooke et al. do not anticipate these dependent claims for the same reasons set forth above in support of the patentability of claim 181.

Withdrawal of this rejection is therefore respectfully requested.

**V. Rejection of Claim 179 Under 35 U.S.C. § 102(e)**

Claim 179 stands rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,857,097 (“Henzinger et al.”). It is respectfully submitted that Henzinger et al. do not anticipate claim 179 for at least the following reasons.

Henzinger et al. are unrelated to the features of separating a control flow graph into a plurality of subgraphs among a plurality of programmable hardware modules. While Fig. 5b of Hensinger et al. shows forming a plurality of graphs, the forming of graphs is not for distribution among programmable hardware modules. Rather, the graphs are formed for analyzing performance of a computer system. See Henzinger et al., column 2, line 18 to column 3, line 15.

Further, nowhere do Henzinger et al. disclose that the decomposition of the augmented control flow graph (Fig. 5a, step 520) described with respect to Fig. 5b, is performed so as to minimize connections between subgraphs. That the particular subgraphs shown in Fig. 5b happen to be such that no connection is shown between them does not indicate that the separation is performed in this manner. Indeed, nowhere do Henzinger et al. disclose, or even suggest, the features of separating a control flow graph into a plurality of subgraphs that are distributed among hardware modules, where the separating includes separating the control flow graph so as to minimize connections between the plurality of subgraphs.

Thus, Henzinger et al. do not disclose, or even suggest, all of the features recited in claim 179. Accordingly, Henzinger et al. do not anticipate claim 179.

Withdrawal of this rejection is therefore respectfully requested.

**VI. Rejection of Claims 190 to 193 Under 35 U.S.C. § 102(e)**

Claims 190 to 193 stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,841,973 (“Kessler et al.”). It is respectfully submitted that Kessler et al. do not anticipate any of claims 190 to 193 for at least the following reasons.

Claim 190 recites transmitting a data signal and a status from a first cell to a second cell in a method of executing a single program on a system having an array of runtime reconfigurable cells.

As set forth in the Amendment dated September 28, 2006, Kessler et al. provide for multiple processors that store data in and retrieve data from memories of each others’ processors. The multiple processors operate in parallel to perform different programs, during which the storing and retrieval may be performed. Kessler et al., however, do not

disclose, or even suggest, that that the storing and retrieving is performed in a method for executing a single program on a system having an array of runtime reconfigurable cells. Thus, Kessler et al. do not disclose, or even suggest, all of the features recited in claim 190.

In the “Response to Argument” section, the Office Action states that the features of “‘a single program on a system having an array of runtime reconfigurable cells’ . . . [has] not been given patentable weight because the recitation occurs in the preamble.” Office Action, page 3. However, the Examiner should have considered these features of the preamble since “clear reliance on the preamble during prosecution to distinguish the claimed invention from the prior art transforms the preamble into a claim limitation.” *Catalina Mktg. Int’l v. Coolsavings.com, Inc.*, 289 F.3d 801, 808-09, 62 U.S.P.Q.2d 1781, 1785 (Fed. Cir. 2002); *M.P.E.P.* § 2111.02.

It is therefore respectfully submitted that Kessler et al. do not anticipate claim 190.

As for claims 191 to 193, which ultimately depend from claim 190 and therefore include all of the features recited in claim 190, it is respectfully submitted that Kessler et al. do not anticipate either of these dependent claims for the same reasons set forth above in support of the patentability of claim 190.

Withdrawal of this rejection is therefore respectfully requested.

## **VII. Rejection of Claims 194 to 202 Under 35 U.S.C. § 102(e)**

Claims 194 to 202 stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 4,972,314 (“Getzinger et al.”). It is respectfully submitted that Getzinger et al. do not anticipate any of claims 194 to 202 for at least the following reasons.

Claim 194 relates to a method of executing a program on a reconfigurable array of cells, and recites the following:

*. . . forming a plurality of subgraphs based on a program;  
computing a first part of a first one of the subgraphs with a first  
cell; after computing, reconfiguring the first cell for computation of  
a first part of a second one of the subgraphs; and simultaneously  
with the reconfiguring, computing a second part of the first  
subgraph with a second cell.*

The cited sections of Getzinger et al. refer to execution of program elements of a graphed program by sequentially loading instances of the program elements (node instances) into a queue as they become ready. When a processing element becomes free, it obtains the first node instance in the queue for execution. After execution, the processing element stores what it has produced in a produce queue. The cited sections do not disclose,

or even suggest, forming a plurality of subgraphs, where different parts of the various subgraphs are executed by multiple cells as provided for in the context of claim 194.

For example, the Office Action asserts that Fig. 6 of Getzinger et al. shows reconfiguring one cell for computing a first part of a one subgraph while a second cell computes a second part of another subgraph, the first part of which has been previously computed by the first cell. It is unclear how the Examiner gleans all these features from the illustration of Fig. 6, which merely shows memory queues including a first queue of node instances to be consumed and a second queue of node instances for which output has been produced. A sequence of execution of parts of different subgraphs, a sequence of execution of subgraph parts in relation to multiple cells, and when cells are reconfigured are all not shown or indicated by Fig. 6. Indeed, it is respectfully submitted that Getzinger et al. do not disclose, or even suggest, these features of claim 194.

Thus, Getzinger et al. do not disclose, or even suggest, all of the features recited in claim 194. Accordingly, Getzinger et al. do not anticipate claim 194.

As for claims 195 to 202, which ultimately depend from claim 194 and therefore include all of the features recited in claim 194, it is respectfully submitted that Getzinger et al. do not anticipate either of these dependent claims for the same reasons set forth above in support of the patentability of claim 194.

Withdrawal of this rejection is therefore respectfully requested.

#### **VIII. Rejection of Claim 194 Under 35 U.S.C. § 102(e)**

Claim 194 stands rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 7,007,096 ("Lisitsa et al."). It is respectfully submitted that Lisitsa et al. do not anticipate claim 194 for at least the following reasons.

The Office Action asserts that Figs. 4A, 4C, 6A, and 6B and the corresponding text of Lisitsa et al. disclose the features of claim 194. However, Lisitsa et al. provide for creating a graph of a flow of data frames between modules and of the mixing and separating of data frames corresponding to the graphed flow of the data frames between the modules. In this regard, Fig. 4A is a graph of a flow starting at modules M4A and M4B and ending at module M4I. Fig. 4C is graph of data frames F401, F401, F404, F405, F412, and F414 as they are passed in between pins of the modules to ultimately form a super-frame F421 by processing performed by module M4H and then be split by module M4I into frames F423 and F424 (corresponding to pins P423 and P424 of module M4I). Each of the graphs is thus a single graph representing a sequential flow of data. Once the graphs are generated, the

modules are statically assigned for execution of corresponding parts of the graph of Fig. 4A. After the assignment, the graph is played. See Fig. 6B and corresponding text. During the execution, downstream modules must wait for upstream modules to complete their tasks for providing the split or mixed data frames to the downstream modules.

Lisitsa et al. do not provide for forming subgraphs of either of the graphs of Figs. 4A and 4C. Further, the modules are not reconfigured during execution for performing different parts of the tasks of the graphs. Each module of Fig. 4A performs a single task. At most, modules of Fig. 4A that have been assigned tasks requiring input from different sets of upstream modules can perform their respective tasks simultaneously and without regard to whether each other's inputs are ready.

Further, with respect to the computation of the different parts of the different subgraphs as provided for in the context of claim 194, the Office Action asserts that F411, F410, and F409 disclose the first part of a second one of the subgraphs and that F420 to F421 discloses the second part of the first subgraph. Applicants fail to understand the Examiner's argument. The block including F411, F410, and F409 represents a data frame F419, which corresponds to pins P409, P410, P411, and P419. The block including F420 and F418 represents a data frame F420, which corresponds to pins P418 and P420. The block including F421 and F422 represents a frame F421 formed by the combination of frames F419 and F420, ***which is generated by a single module M4H***. These blocks do not show different parts of different subgraphs computed by different cells.

Thus, Lisitsa et al. do not disclose, or even suggest, all of the features recited in claim 194. Accordingly, Lisitsa et al. do not anticipate claim 194.

Withdrawal of this rejection is therefore respectfully requested.

#### **IX. Rejection of Claim 180 Under 35 U.S.C. § 103(a)**

Claim 180 stands rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of U.S. Patent No. 5,021,947 ("Campbell et al.") and U.S. Patent No. 6,311,265 ("Beckerle et al."). It is respectfully submitted that the combination of Campbell et al. and Beckerle et al. does not render unpatentable claim 180 for at least the following reasons.

Claim 180 relates to a method for programming a system having a cellular structure and recites, *inter alia*, the following:

*. . . separating the data flow graph into a plurality of subgraphs;  
and distributing the plurality of subgraphs among a plurality of  
hardware modules; wherein the separating includes separating the*

*data flow graph so as to minimize connections between the plurality of subgraphs.*

The Office Action admits that Campbell et al. do not disclose these features and instead refers to Beckerle et al. as assertedly disclosing these features. The cited section of Beckerle et al. provides examples of program graph components that may be created by a user via a user interface. The cited section indicates that some such components might be a graph of parallel processing independently performed. The cited section does not refer to separating a program graph into subgraphs that are distributed among hardware modules, and certainly does not disclose such separating performed so as to minimize connections between the subgraphs being distributed.

Thus, the combination of Campbell et al. and Beckerle et al. does not disclose or suggest all of the features recited in claim 180. Accordingly, the combination of Campbell et al. and Beckerle et al. does not render unpatentable claim 180.

Withdrawal of this rejection is therefore respectfully requested.

**X. Rejection of Claims 183, 184, and 186 Under 35 U.S.C. § 103(a)**

Claims 183, 184, and 186 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Cooke et al. and U.S. Patent No. 6,421,809 (“Wuytack et al.”). Without addressing whether Wuytack et al. qualifies as prior art with respect to the sections of Wuytack et al. relied upon by the Examiner, it is respectfully submitted that the combination of Cooke et al. and Wuytack et al. does not render unpatentable any of claims 183, 184, and 186 for at least the following reasons.

Claims 183, 184, and 186 depend from claim 181 and therefore include all of the features recited in claim 181. Wuytack et al. do not correct the deficiencies noted above with respect to Cooke et al. It is therefore respectfully submitted that the combination of Cooke et al. and Wuytack et al. does not render unpatentable these dependent claims for the same reasons set forth above in support of the patentability of claim 181. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988) (any dependent claim that depends from a non-obvious independent claim is non-obvious).

Withdrawal of this rejection is therefore respectfully requested.

**XI. Rejection of Claim 189 Under 35 U.S.C. § 103(a)**

Claim 189 stands rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Cooke et al. and U.S. Patent No. 6,301,706 (“Maslennikov et al.”). It is respectfully submitted that the combination of Cooke et al. and Maslennikov et al. does not render unpatentable claim 189 for at least the following reasons.

Claim 189 depends from claim 181 and therefore includes all of the features recited in claim 181. Maslennikov et al. do not correct the deficiencies noted above with respect to Cooke et al. It is therefore respectfully submitted that the combination of Cooke et al. and Maslennikov et al. does not render unpatentable this dependent claim for the same reasons set forth above in support of the patentability of claim 181. *Id.*

Withdrawal of this rejection is therefore respectfully requested.

**XII. Rejection of Claim 203 Under 35 U.S.C. § 103(a)**

Claim 203 stands rejected under 35 U.S.C. § 103(a) as unpatentable over the combination of Cooke et al. and Wuytack et al. Without addressing whether Wuytack et al. qualifies as prior art with respect to the sections of Wuytack et al. relied upon by the Examiner, it is respectfully submitted that the combination of Cooke et al. and Wuytack et al. does not render unpatentable claim 203 for at least the following reasons.

Claim 203 relates to a method for programming a system having a cellular structure and, as amended herein without prejudice, recites, *inter alia*, the following:

*. . . extracting from a program at least one of a data flow graph and a control flow graph . . . wherein:  
the extracting includes, for a conditional instruction of the program, extracting a plurality of different subgraphs, each representing a different instruction path of the conditional instruction, the conditional instruction indicating which of the executed instruction paths is to be selected for providing output of the selected instruction path to a further subgraph; and  
for each one of the different subgraphs, the system sets execution of the subgraph to be bypassed as soon as an evaluation in accordance with the conditional instruction reveals that output of the subgraph will not be selected.*

The Office Action admits that Cooke et al. do not disclose for a conditional instruction, extracting a plurality of different subgraphs, each representing a different instruction path of the conditional instruction, or that for each of the different subgraphs, execution is dependent on an evaluation of the conditional instruction, but instead refers to Wuytack et al. as assertedly disclosing these features.

However, while Wuytack et al. might suggest that loops are executed depending on the conditional statements a program specifies for determining whether to perform the steps of the loop, *i.e.*, program instructions written at the heads of the loops, nowhere do Wuytack et al. disclose or suggest a system that sets execution of a subgraph that represents an instruction path of a conditional instruction to be bypassed as soon as an evaluation in accordance with the conditional instruction reveals that the subgraph's output will not be selected, where the program's conditional instruction is one that refers to the selection of output of an executed instruction path.

Thus, the combination of Cooke et al. and Wuytack et al. does not disclose or suggest all of the features recited in claim 203. Accordingly, the combination of Cooke et al. and Wuytack et al. does not render unpatentable claim 203.


Withdrawal of this rejection is therefore respectfully requested.

### **XIII. Conclusion**

In light of the foregoing, it is respectfully submitted that all pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully submitted,

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By:   
Michelle Carniaux  
Reg. No. 36,098

KENYON & KENYON LLP  
One Broadway  
New York, New York 10004  
(212) 425-7200  
CUSTOMER NO. 26646